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1. In a data processing system having a system bus and having a processor with a level one cache memory responsively coupled to a level two cache memory which is responsively coupled to a level three memory, said level two cache memory having cache storage and tag storage and having a circuit for SNOOPing said system bus , the improvement comprising:

a. A first dedicated path between said system bus and said cache storage and a second dedicated path between said system bus and said tag storage.

2. A data processing system according to claim 1 further comprising control logic responsively coupled to said cache storage and said tag storage which provides the highest priority for said SNOOPing.

3. A data processing system according to claim 2 wherein said level two cache memory further comprises:

a. A duplicate tag memory.

4. A data processing system according to claim 3 further comprising:

a. A plurality of instruction processors.

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5. A data processing system according to claim 4 wherein said level three memory further comprises:

a. A level three cache memory.

6. A data processing system comprising:

a. A processor having a level one cache memory;

b. A level two cache memory having a data memory and a tag memory responsively coupled to said level one cache memory;

c. A system memory bus responsively coupled to said data memory and responsively coupled to said tag memory; and

d. A SNOOP request placed on said system memory bus and responsively coupled to said tag memory.

7. A data processing system according to claim 6 further comprising:

a. A data request transferred from said level one cache memory to said level two cache memory.

8. A data processing system according to claim 7 further comprising:

a. Control logic within said level two cache memory which provides priority of said SNOOP request over said data request.

9. A data processing system according to claim 8 further comprising:

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a. A level one tag memory located within said level one cache memory; and

b. A duplicate tag memory within said level two cache memory which maintains a duplicate of information within said level one tag memory.

10. A data processing system according to claim 9 wherein said SNOOP request is responsively coupled to said duplicate tag memory.

11. A method of maintaining validity of data within a level one cache memory of a processor having a level one tag memory responsively coupled to a level two cache memory having a tag memory and a data memory wherein said level two cache memory is responsively coupled to a system memory bus comprising:

a. Formulating a SNOOP request;

b. Presenting said SNOOP request on said system memory bus to said level two cache memory;

c. Routing said SNOOP request directly to said tag memory; and

d. Processing said SNOOP request.

12. A method according to claim 11 further comprising:

a. Presenting a data request from said level one cache memory to said level two cache memory; and

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b. Granting priority to said SNOOP request over said data request.

13. A method according to claim 12 further comprising:

a. Maintaining a duplicate copy of said level one tag memory within a duplicate tag memory within said level two cache memory.

14. A method according to claim 13 further comprising:

a. Routing said SNOOP request to said duplicate tag memory.

15. A method according to claim 14 further comprising:

a. Processing said SNOOP request regarding said duplicate tag memory.

16. An apparatus comprising:

a. Means for executing program instructions;

b. Means responsively coupled to said executing means for level one caching data;

c. Means responsively coupled to said executing means and said level one caching means for requesting a data element if said executing means requires requesting of said data element and said level one caching means does not contain said data element;

d. Means responsively coupled to said requesting means for level two caching;

e. Means located within said level two caching means for

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storing level two caching data;

f. Means located within said level two caching means for maintaining level two tags; and

g. Means responsively coupled to said maintaining means for directly SNOOPing said level two tag1.

17. An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said storing means and said maintaining means for granting priority to a SNOOP request over said data element request.

18. An apparatus according to claim 17 further comprising:

a. Means responsively coupled to said level two caching means for bussing system memory data;

b. Means responsively coupled to said bussing means for interfacing said bussing means directly to said storing means; and

c. Means responsively coupled to said bussing means for interfacing said bussing means directly to said maintaining means.

19. An apparatus according to claim 18 further comprising:

a. Means located within said level one caching means for recording level one tags; and

b. Means located within said level two caching means and responsively coupled to said recording means for duplicating said level one tags.

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20. An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said bussing means and said duplicating means for SNOOPing said duplicating means.